

# Zero Chirp Tunable SFP+ 10G Serial Optical Transceiver

TRS7091FNCDP000-X



The Lumentum tunable SFP+ optical transceiver is a high-performance tunable pluggable transceiver for use in the C-band window covering 1528 nm to 1566 nm. The module supports data rates from 9.95 Gbps to 11.3 Gbps and is provided in an SFP+, MSA-compliant package.

The optical transmitter utilizes the Lumentum tunable ILMZ chip to provide a high performance, low cost 10G transceiver. Channel tuning is supported on the ITU-T 50 GHz grid across full C band with  $\pm 2.5$  GHz stability. Wavelength and frequency tuning modes are supported in accordance with SFF-8690.

The receive path comprises a PIN PD receiver with CDR.

Mechanical dimensions, connectors and footprint conform to SFP+ MSA. The module size is 56.5 mm L x 13.9 mm W x 11.85 mm H with 20-pin electrical connector. The maximum power consumption is 2.0 W at 70°C, and power supply voltage is +3.3 V.

#### Key Features

- 1550 nm ITU-T C-band 50 GHz spacing tunable DWDM SFP+ optical transceiver
- Data rate 9.95-11.3 Gbps
- Support  $\pm 700$  ps/nm dispersion
- Zero chirp transmitters with ILMZ TOSA
- PIN PD receiver with CDR
- Low power consumption: <2.0 W at 70°C
- Positive power supply lines: 3.3 V
- Operating case temperature range: 0°C to 70°C
- Compact size (56.5 mm L x 13.9 mm W x 11.85 mm H)

#### Compliance

- SFF-8431 – Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module (SFP+)
- SFF-8432 - Improved Pluggable Form factor
- SFF-8690 - Tunable SFP+ Memory Map for ITU Frequencies
- SFF-8472 - Diagnostic Monitoring Interface for Optical Xcvrs
- INF-8074i - SFP (Small Form Factor) Transceiver
- IEEE802.3ae CL 52 - IEEE 802.3 Standard (10Gigabit Ethernet Clause)
- MIL-STD-883, Method 3015.4
- IEC61000-4-2:Edition1 (Air Discharge)
- Class 1 Laser Safety

FUNCTIONAL DESCRIPTION

1. SFI Data Interface

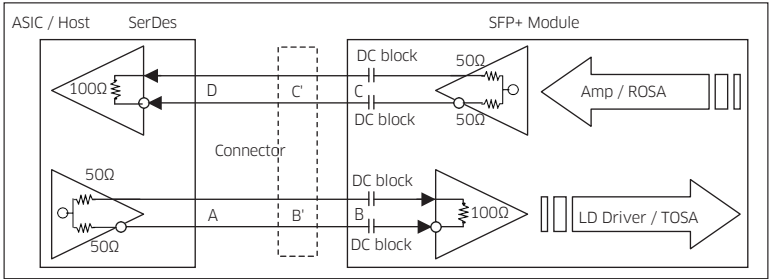


Figure 1 Interface to host

Table 1: SFP+ Module Transmitter Electrical Characteristics at B''

Parameter @ B''	Symbol	Minimum	Maximum	Units
Eye mask	X1		0.12	UI
Eye mask	X2		0.33	UI
Eye mask	Y1	95		mV
Eye mask	Y2		350	mV

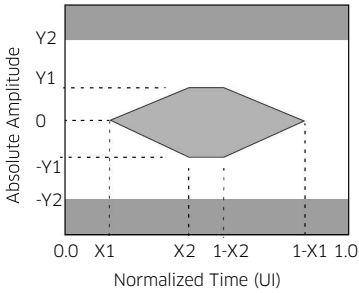


Figure 2 Eye mask at B''

Table 2: SFP+ Module Receiver Electrical Characteristics at C'

Parameter @ C'	Symbol	Minimum	Maximum	Units
Eye mask	X1		0.35	UI
Eye mask	Y1	150		mV
Eye mask	Y2		425	mV

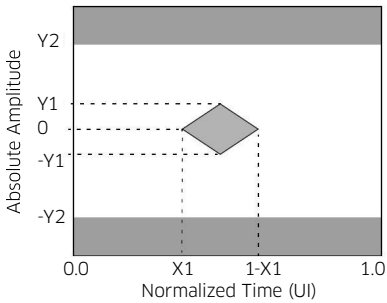


Figure 3 SFP+ eye mask at C'

## 2. Low Speed Control Pins

- TX\_Fault
- TX\_Disable
- Mod\_ABS
- RX\_LOS

**Table 3: Low Speed Control Pin Logic Levels**

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Host VCC Range	Host_V <sub>CC</sub>	3.14	3.47	V	With ± 5% variation
TX_Fault, RX_LOS	V <sub>OL</sub>	0.0	0.40	V	Note 1
	V <sub>OH</sub>	Host_V <sub>CC</sub> - 0.5	Host_V <sub>CC</sub> + 0.3	V	Note 1
TX_Disable	V <sub>IL</sub>	-0.3	0.8	V	Pulled up with 10k ohms to V <sub>CC</sub> T in the module.
	V <sub>IH</sub>	2.0	V <sub>CC</sub> T + 0.3	V	

Note:

1. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measured at the Host side of the connector.

**TX\_Fault** is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety. The TX\_Fault output pin is an open drain/collector and must be pulled up to the Host\_Vcc with 4.7k-10k  $\Omega$  on the host board

**TX\_Disable** is a module input pin. When TX\_Disable is asserted High or left open, the SFP+ module transmitter output must be turned off. The TX\_Disable pin is pulled up to V<sub>CC</sub>T with 10k  $\Omega$  in the SFP+ module. The TX\_Disable pin works for TX\_fault\_Reset as well.

**Mod\_ABS** is pulled up to Host\_V<sub>CC</sub> with 4.7k-10k  $\Omega$  on the host board and connected to VeeT or VeeR in the SFP+ module. Mod\_ABS is then asserted "High" when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD\_DEFO.

**RX\_LOS** when high indicates an optical signal level below that specified in the relevant standard. The RX\_LOS pin is an open drain/collector output and must be pulled up to host V<sub>CC</sub> with a 4.7k-10k $\Omega$  on the host board. RX\_LOS assert min and de-assert max are defined in the relevant standard.

3. 2-Wire Interface I<sup>2</sup>C: SDA & SCL

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up with a voltage in the range of 3.14 V to 3.47 V on the host. SFP+ low speed interface is based on 2-wire interface. SFP+ 2-Wire interface is based on Low Voltage TTL (LVTTTL) operating with a supply of 3.3 V ±5% and are given in Table 4. This specification ensures compatibility between host masters and SFP+ SCL/SDA lines and compatibility with I<sup>2</sup>C. All voltages are referenced to V<sub>ee</sub>T.

Note: After an interruption in protocol, power loss or system reset, the 2-wire part can be reset by following these steps:  
1. Clock up to 9 cycles.  
2. Look for SDA high in each cycle while SCL is high.  
3. Create a start condition.

Table 4: 2-Wire Interface Physical Interface

Parameter	Symbol	Min.	Max.	Unit	Conditions
Host V <sub>cc</sub> range	Host_V <sub>cc</sub>	3.14	3.47	V	
SCL and SDA	V <sub>OL</sub>	0.0	0.40	V	R <sub>pullup</sub> <sup>1</sup> pulled to Host_V <sub>cc</sub> IOL(max) = 3 mA
	V <sub>OH</sub>	Host_V <sub>cc</sub> - 0.5	Host_V <sub>cc</sub> + 0.3	V	R <sub>pullup</sub> <sup>1</sup> pulled to Host_V <sub>cc</sub>
SCL and SDA	V <sub>IL</sub>	-0.3	V <sub>cc</sub> T + 0.5	V	
	V <sub>IH</sub>	V <sub>cc</sub> T * 0.7	10	μA	
Input current on SCL and SDA pins	I <sub>L</sub>	-10	10	μA	
Capacitance on SCL and SDA pins	C <sub>i</sub> <sup>2</sup>		14	pF	
Total bus capacitance for SCL and SDA	C <sub>b</sub> <sup>3</sup>		100	pF	At 400 kHz, R <sub>p</sub> (max) = 3.0 kΩ At 100 kHz, R <sub>p</sub> (max) = 8.0 kΩ
			290	pF	At 400 kHz, R <sub>p</sub> (max) = 1.1 kΩ At 100 kHz, R <sub>p</sub> (max) = 2.75 kΩ

Note:  
1. R<sub>pullup</sub> (R<sub>p</sub>) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measured at the Host side of the connector. V<sub>cc</sub>T/R + 0.5 V nor requires the module to sink more than 3.0 mA current.  
2. C<sub>i</sub> is the capacitance looking into the module SCL and SDA pins  
3. C<sub>b</sub> is the total bus capacitance on the SCL or SDA bus

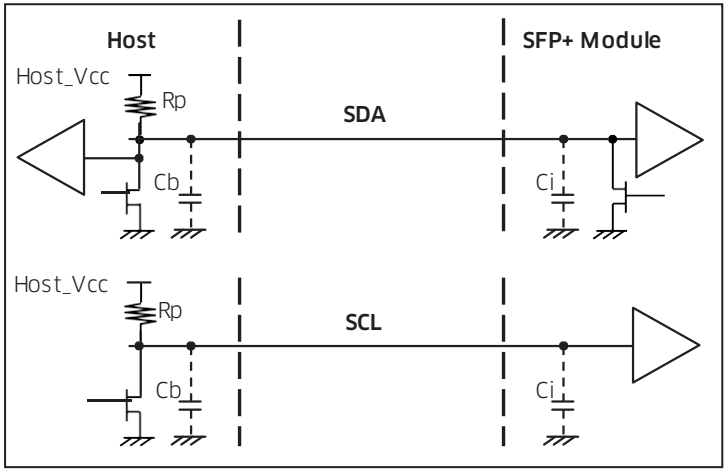


Figure 4 2-Wire interface physical interface

**Table 5: SFP+ 2-Wire Interface Timing Requirements**

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Clock frequency	$f_{SCL}$	100	400	kHz	
Clock pulse width low	$t_{LOW}$	1.3		$\mu s$	
Clock pulse width high	$t_{HIGH}$	0.6		$\mu s$	
Time bus free before new transaction can start	$t_{BUF}$	20		$\mu s$	Between STOP and START
START hold time	$t_{HD,STA}$	0.6		$\mu s$	
START set-up time	$t_{SU,STA}$	0.6		$\mu s$	
Data in hold time	$t_{HD,DAT}$	0		$\mu s$	
Data in set-up time	$t_{SU,DAT}$	0.1		$\mu s$	
Input rise time (100 kHz)	$t_{R,100}$		1000	ns	Note 1
Input rise time (400 kHz)	$t_{R,400}$		300	ns	Note 1
Input fall time (100 kHz)	$t_{F,100}$		300	ns	Note 1
Input fall time (400 kHz)	$t_{F,400}$		300	ns	Note 1
STOP set-up time	$t_{SU,STO}$	0.6		$\mu s$	
Serial interface clock holdoff "clock stretching"	$T_{clock\_hold}$		500		Maximum time the SFP+ may hold the SCL line low before continuing R or W operation
Complete single or sequential write	$t_{WR}$		40	ms	Complete (up to) 8 Byte write
Endurance (write cycles)		10 k		Cycles	@ Max operating temperature

Note:  
1. From  $(V_{IL,MAX} - 0.15)$  to  $(V_{IH,MIN} + 0.15)$

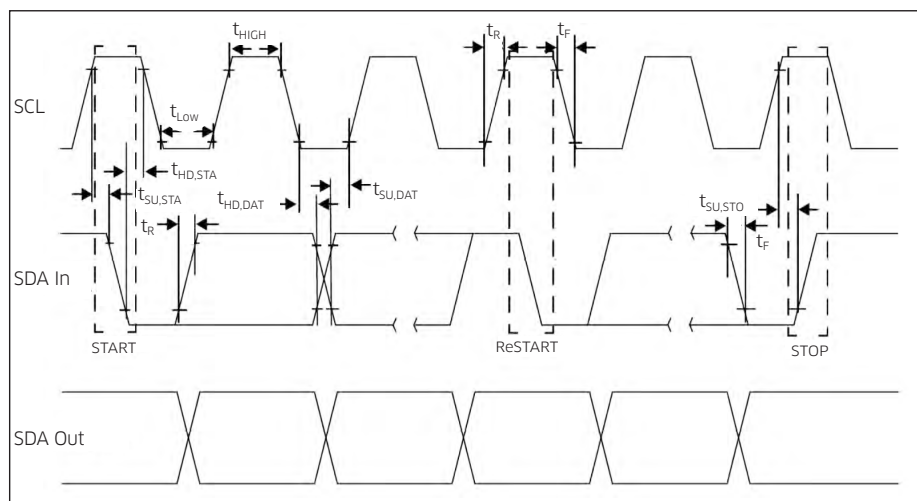


Figure 5 SFP+ timing diagram

#### 4. SFP+ Module Timing

In the below figures are shown the required timing for TX\_Fault and TX\_Disable in various conditions. For more detail, please refer to SFF-8431.

**Table 6: SFP+ Timing Requirements**

Parameter	Symbol	Min	Max	Unit	Conditions
TX_disable assert time	t_off		100	μs	Rising edge of TX_disable to fall of output signal below 10% of nominal.
TX_disable negate time	T_on		2	ms	Falling edge of TX_disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 9.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	sec	From power supplies meeting Table 9 or hot plug, or Tx_disable negated during power up or Tx_fault recovery, until cooled power level II part during fault recovery is fully operational. Also, from stop bit low-to-high SDA transition enabling power level II until cooled module is fully operational
Tx_fault assert for cooled module	Tx_fault_on_cooled		1	ms	From occurrence of fault to assertion of TX_Fault
Tx_fault_reset	t_reset	10		μs	Time TX_disable must be held high to reset TX_Fault.
RX_LOS assert delay	t_los_on		100	μs	From occurrence of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_los_off		100	μs	From occurrence of presence of signal to negation of RX_LOS

#### 5. Maximum Current Ramp on Power supply

In the below figure and table are shown the required inrush current characteristics for the module power pins.

**Table 7: Inrush Current**

Parameter	Symbol	Min.	Max.	Unit	Remarks
Icc instantaneous peak current			600	mA	Note 1, 2
Icc sustained peak current			500	mA	Note 1, 2

Note:

1. The maximum currents are the allowed currents for each power supply VccT or VccR, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period.

2. Not to exceed the sustained peak limit for more than 50 μs; may exceed this limit for shorter durations

## PERFORMANCE SPECIFICATIONS

### Absolute Maximum Ratings

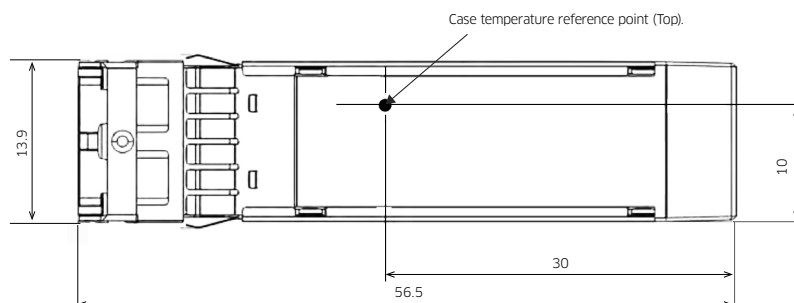
Stresses in excess of the absolute maximum ratings can cause permanent damage to the transceiver.

**Table 8: Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Unit	Remarks
Supply voltage	$V_{CC}T$	0	+3.6	V	+3.3 V
Supply voltage	$V_{CC}R$	0	+3.6	V	+3.3 V
Optical receiver input	$P_{IMAX}$		+5	dBm	Average
Operating case temperature	$T_c$	-10	+75	°C	Note 1
Storage temperature	$T_{STR}$	-40	+85	°C	
ESD SFI pins	ESD1		1	kV	HBM
ESD except for SFI pins	ESD2		2	kV	HBM

Note:

1. Case temperature reference point is shown below



### Operating Environment

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

**Table 9: Operating Environment**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Supply voltage	$V_{CC}T$	3.135	3.300	3.465	V	+3.3 V
Supply voltage	$V_{CC}R$	3.135	3.300	3.465	V	+3.3 V
Operating case temperature	$T_c$	0	25	+70	°C	

### Electrical Performance

**Table 10: Power Supply Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Supply voltage	$V_{CC}T$	3.135	3.300	3.465	V	
	$V_{CC}R$	3.135	3.300	3.465	V	
Operating case temperature	$I_{CC3}$			0.63	A	Note 1
	$P_{DS}$			2.0	W	Note 2

Notes:

1. <0.67 A  $T_c < 5^\circ\text{C}$

2. <2.1 W  $T_c < 5^\circ\text{C}$



**Optical Interface Characteristics****Table 11 Optical Characteristics**

Parameter	Symbol	Min.	Typ	Max	Unit	Remarks
<b>Transmitter</b>						
Data rate		9.95		11.3	Gbit/s	NRZ
Frequency range		191.30		196.05	THz	50 GHz grid, 96 channels
Frequency accuracy		-2.5		+2.5	GHz	EOL
Optical transmit power	Po	-2.0		+3.0	dBm	EOL
Shuttered output power				-35	dBm	
Optical power stability	$\Delta P_o$	-1.0		+1.0	dB	All channels, SOL
Side mode suppression	SMSR	35			dB	$\pm 2.5$ nm, modulated
Spectral width	$\Delta\lambda$		0.3	0.5	nm	-20 dB, modulated
Extinction ratio	ER	9.0			dB	Filtered, 10.709 Gbps
Eye diagram compliance		GR-253, ITU-T G.691				
Mask margin		10			%	
<b>Receiver</b>						
Data rate		9.95		11.3	Gbit/s	NRZ
Input operating wavelength		1525		1575	nm	
Minimum receiver sensitivity (back to back)	Prmin			-14	dBm	10.709 Gbps, 1E-12, OSNR>35 dB
Maximum input power (overload)	Pro	0			dBm	
Receiver reflectance	RL	-27			dB	
LOS assert		-27			dBm	
LOS de-assert				-20	dBm	
LOS hysteresis		0.5		4.0	dB	
LOS assert time				100	us	
LOS de-assert time				100	us	

**System Performance****Table 12 System Performance**

Parameter	Dispersion	OSNR Resolution BW 0.1nm	BER	Remarks
OSNR dispersion tolerance	-700 ps/nm	17 dB	1E-04	10.709 Gbps, -3 to -14 dBm, -0.25 nm filter BW, Rx DTV optimized
	0 ps/nm	15 dB	1E-04	
	700 ps/nm	17 dB	1E-04	

**Jitter Characteristics****Table 13 Transmitter Jitter Characteristics (Note 1)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Jitter peaking				0.03	dB	
				1	dB	frequency > 120 kHz
Module Jitter Generation at Optical Output				100	mUIpp	4 MHz to 80 MHz
				300	mUIpp	20 MHz to 80 MHz

Note:

1. Data Rate; NRZ at 9.953 Gbps, SONET framed PRBS=2<sup>31</sup>-1 data Jitter Characteristics

**Table 14 Receiver Jitter Characteristics (Note 1)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Jitter peaking				0.03	dB	
				1	dB	frequency > 120 kHz
Jitter tolerance		Figure 7				

Note:

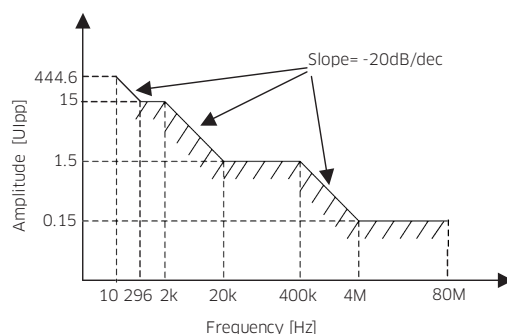
1. Data rate; NRZ at 9.953 Gbps, SONET framed PRBS=2<sup>31</sup>-1 data

Figure 6 Jitter tolerance

**Pin out Definition****Table 15: Pin Description**

Pin	Logic	Symbol	Power Sequence Order	Name/Description	Notes
1		VeeT	1 <sup>st</sup>	Module transmitter ground	1
2	LVTTL-O	TX_Fault	3 <sup>rd</sup>	Module transmitter fault	2
3	LVTTL-I	TX_Disable	3 <sup>rd</sup>	Transmitter disable; turn off laser output	3
4	LVTTL-I/O	SDA	3 <sup>rd</sup>	2-wire serial interface data line	4
5	LVTTL-I/O	SCL	3 <sup>rd</sup>	2-wire serial interface clock	4
6		Mod_Abs	3 <sup>rd</sup>	Module absent, connected to VeeT or VeeR in the module	5
7	LVTTL-I	RS0	3 <sup>rd</sup>	NA. 30 kohm pull down inside the module	
8	LVTTL-O	RX_LOS	3 <sup>rd</sup>	Receiver loss of signal indicator	2
9	LVTTL-I	RS1	3 <sup>rd</sup>	NA. 30 kohm pull down inside the module	
10		VeeR	1 <sup>st</sup>	Module receiver ground	1
11		VeeR	1 <sup>st</sup>	Module receiver ground	1
12	CML-O	RD-	3 <sup>rd</sup>	Receiver inverted data output(SFI)	
13	CML-O	RD+	3 <sup>rd</sup>	Receiver non-inverted data output(SFI)	
14		VeeR	1 <sup>st</sup>	Module receiver ground	1
15		VccR	2 <sup>nd</sup>	Module receiver 3.3V supply	6
16		VccT	2 <sup>nd</sup>	Module transmitter 3.3V supply	6
17		VeeT	1 <sup>st</sup>	Module transmitter ground	1
18	CML-I	TD+	3 <sup>rd</sup>	Transmitter non-inverted data output(SFI)	
19	CML-I	TD-	3 <sup>rd</sup>	Transmitter inverted data output(SFI)	
20		VeeT	1 <sup>st</sup>	Module transmitter ground	1

Note:

1. The module signal ground pins, VeeR and VeeT, are isolated from the module case.

2. This pin is an open drain output pin and shall be pulled up with 4.7 k-10 kohms to Host\_Vcc (Table3) on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.

3. This pin is an input pin with 10kohms pull up to VccT in the module.

4. See table 4 and 5: 2-Wire Electrical Specifications .

5. This pin shall be pulled up with 4.7 k-10 kohms to Host\_Vcc on the host board.

6. VccT and VccR are tied together inside the module.

## Mechanical

Comply to SFF-8432, the improved Pluggable form factor specification, with technique #2 latch.

Comply to optional operational mechanical shock test in issue 2 of GR468.

## Optical Connector

LC Connector

## RoHS

RoHS compliant per Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast).

## Mechanical Dimensions and label location

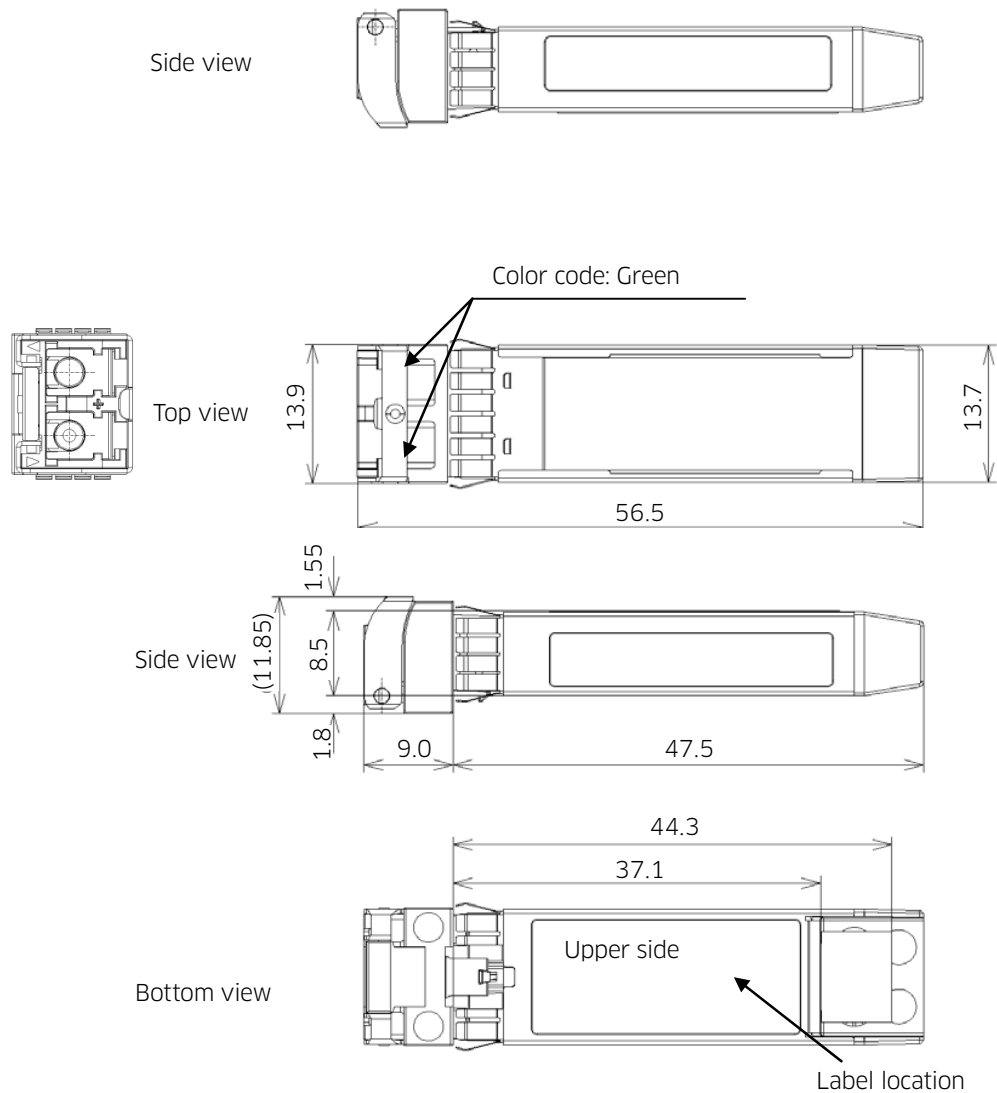


Figure 7 Mechanical dimensions and label location

